ETAPS Daily

Number 7

Friday, April 4

March 29-April 6, 2008, Budapest, Hungary

INVITED TALK

From **09:00**, Michael Schwartzbach presents his talk titled as *Design Choices in a Compiler Course - or - How to Make Undergraduates Love Formal Notation* in the **Star Auditorium**.

Michael Schwartzbach is an Associate Professor at the University of Aarhaus, Denmark where he got his PhD in Copmputer Science in 1987. He his research interests include programming languages (design, implementation, and analysis), applications of monadic second-order logic, Web technology and XML.

ANNOUNCEMENTS

The following contributions were selected for this year's best paper awards:

Kenneth McMillan (Cadence Berkeley Labs, USA): *Generating Quantified Invariants with an Interpolating Saturation Prover* (EASST)

Junghee Lim and **Thomas Reps** (University of Wisconsin-Madison, USA): *A System for Generating Static Analyzers for Machine Instructions* (EAPSL)

Christel Baier (Dresden Technical University, Germany), **Nathalie Bertrand** (IRISA Rennes, France) and **Marcus Groesser** (Dresden Technical University, Germany): *On Decision Problems for Probabilistic Buechi Automata* (EATCS).

Paphos, Cyprus was selected as the location of **ETAPS 2010** (March 20-28). Organization will be run by the *Department of Computer Science, University of Cyprus*.

INTERVIEWS

Yesterday the first invited talk was given by **Sharad Malik** on *Hardware Verification: Techniques, Methodology and Solutions* introducing a formal and generalized concept of *microarchitecture*, a layer between high level specification and block diagrams (RTL).

ETAPS Daily: How is this different from the concept of microarchitecture that exists for microprocessors.

Sharad Malik: The notions of architecture and microarchitecture in the processor domain are informal and thus cannot be generalized to all of hardware design. The models I presented cover this gap and show their value in verification.

E.D.: What are the typical errors in the design step from the architectural to RTL level?

SM: The errors typically have to do with the misunderstanding of interactions of concurrent components. Things are very nice when sequential but as soon as you get to concurrent interaction it becomes harder and that typically leads to errors.

E.D: What is the difference between verification of the step from the architecture to microarchitecture and the one from microarchitecture to RTL level?

S.M.: The first problem is similar to what we have today in verification of the step from the architectural level to RTL except that, hopefully, by reducing the gap and making information more explicit in the models the problem is simplified.

Between the bottom two levels, if you can take the microarchitecture and synthesize it down to the block level, then, because you know what you are allowed to do in the synthesis, you can create a simpler verification problem. We already do that when we go from block level to gate level and the same idea can be applied for the next two levels between microarchitecture to RTL. So it is a limited problem because you are starting with limited degrees of freedom.

E.D.: Which could be a "next level of value for formal methods" you mentioned?

S.M.: First, this kind of modeling then makes the verification problems simpler. So I am hoping that we can use formal techniques to take these simpler problems and solve them more effectively.

I also think there is value in seeing complementary techniques where we do offline and online verification combined. For instance, we can simplify proofs by assume guarantee reasoning where in offline verification we assume some properties which have to be guaranteed at runtime.

E.D.: What are your current projects?

S.M.: I have one project on runtime verification, we are looking at a variety of problems in multiple processors, and also we are trying to generalize our results.

On the modeling part we are building the tools and a language for specifying complex systems. As I believe it is very important to plug in to the existing flows, we start with Verilog (a HW description language) and we are adding transaction support and support for integrating the two levels on top of Verilog. It is an extension of Verilog and the best way to think about it is like going from C to C++, with the difference that we also

remove some elements. Therefore it is more like "Verilog+-".

The second invited talk was presented by **Igor Walukiewicz** titled *Finding your way in a forest: on different types of trees and their properties.*

ETAPS Daily: What you think were the most important results related to understanding logics trees in the last couple of years?

Igor Walukiewicz: There were attempts in the 80s and early 90s on the definability problem that turned to be too difficult at that time. The subject came back a few years ago and it looks now it is going to stay for some time.

E.D.: What do you see as the most important open questions that you would like to tackle in this area?

I.W.: The Holy Grail is the first-order definability question which is would be a version of Schützenberger theorem for trees. It looks like we are far away from there. We can try with fragments of CTL or first order logic (this is what happens now).

E.D.: It was also interesting to see in your talk that classical logic was captured with variants of CTL, CTL-*, etc. How do these areas interrelate?

I.W.: The idea is very old, LTL vs FOL come from Kamp's theorem in 68. The question is how far this idea can be pushed and what logics can be captured in this way. Once you see Kamp's result, you find it quite natural to try to capture quantification with a finite set of operators. Also in universal algebra you find varieties generated from a finite set of algebras using the wreath product. This is very closely related to Kamp's theorem and its variants.

E.D.: How do you see logics for trees will evolve?

I.W.: For simple trees I think we have enough formalism. But then for trees with data it is absolutely not obvious, there are some proposals in recent years but it is very difficult to find decidable formalisms. Fortunately, it remains a lot to be understood.

WEATHER FORECAST

Friday:

Partly Cloudy. 15°C (59 F)/4°C (39 F)

Saturday:

Cloudy, Light Showers 13°C (57 F)/3°C (37 F)

PROGRAMME

	Room	Ybl (Grand)	Star (Thermal)	Magnolia (Thermal)
9:00	Session 1	Invited talk (Star)		
9:30				CMCS
10:00		Coffee		
10:30		CC	FOSSACS	
11:00	Session 2			CMCS
11:30				
12:00				
12:30	Lunch			
13:00				
13:30				CMCS
14:00	Session 3			
14:30		CC	FOSSACS	
15:00				
15:30				
16:00				
16:30	Session 4	Coffee		CMCS
17:00		CC	FOSSACS	
17:30				
18:00				CMCS SC
18:30	Evening			
19:00				

CULTURE

The National Dance Theatre situated in the Castle District presents *Hungarian Carmen*, a Central-European version of the famous story (nemzetitancszinhaz.hu).

In the palace of Arts (mupa.hu) you can enjoy a jazz concert *To the Memory of Jackie Orszáczky* performed by Jackie Orszaczky Band and guests (Australia).

The *Blonde Hurricane* offers a comedy from one of the Hungarian "pop" writers of the 20th century, Jenő Rejtő (in the Hungarian National Theatre, nemzetiszinhaz.hu).

The Hungarian Opera House presents *Tosca* (in Italian, see opera.hu).

QUIZ

Find the odd one out in the following list:

What makes it different?

Ballpoint pen, safety match, carburetor, lighter, dynamo, railway electrification system, hologram.

Editor: László Gönczy, Budapest University of Technology and Economics, gonczy@mit.bme.hu